

## UMA (11.6")

## Intel Brasswell-M Platform Block Diagram

Charger	PG.30
+3VS5/+5VS5	PG.31
DDR3L	PG.32
MOIC	PG.33
CPU Core	PG.34,35

DDR3L	1600MT/s
Memory down*4pcs	Channel A
PG.14	
DDR3L	1600MT/s
Memory down*4pcs	Channel B
PG.15	

Intel Brasswell

Power : 4.5 (Watt)

Package : BGA1170

Size : 25 X 27 (mm)

PG.2~13

eMMC 4.51

eMMC  
32G/64G  
/128GB PG.24

PCI-E x2

Card Reader  
RTS5239-GR

PG.21

WLAN  
BT COMBO  
NGFF M2 PG.27KBC  
IT8987

PG.28

KB

PG. 23

TP

PG. 23

ROM

PG. 28

LPC

Fast SPI

Azalia

AUDIO  
CODEC  
ALC 3227

PG.19

Speaker

PG.19

Hp

Combo Jack

PG. 20

MIC

eDP (2 lane)

EDP to LVDS

PG.16

LCD connector

PG.17

DP Port0

HDMI

PG.18

USB 3.0

USB 2.0

USB 2.0

Touch  
Screen

PG.17

Webcam

PG.18

USB 2.0

USB 2.0 Hub

PG.26

USB2.0 Port  
X1

PG.24

WLAN  
BT COMBO  
NGFF M2

PG.27

WWAN(Optional)  
NGFF M2

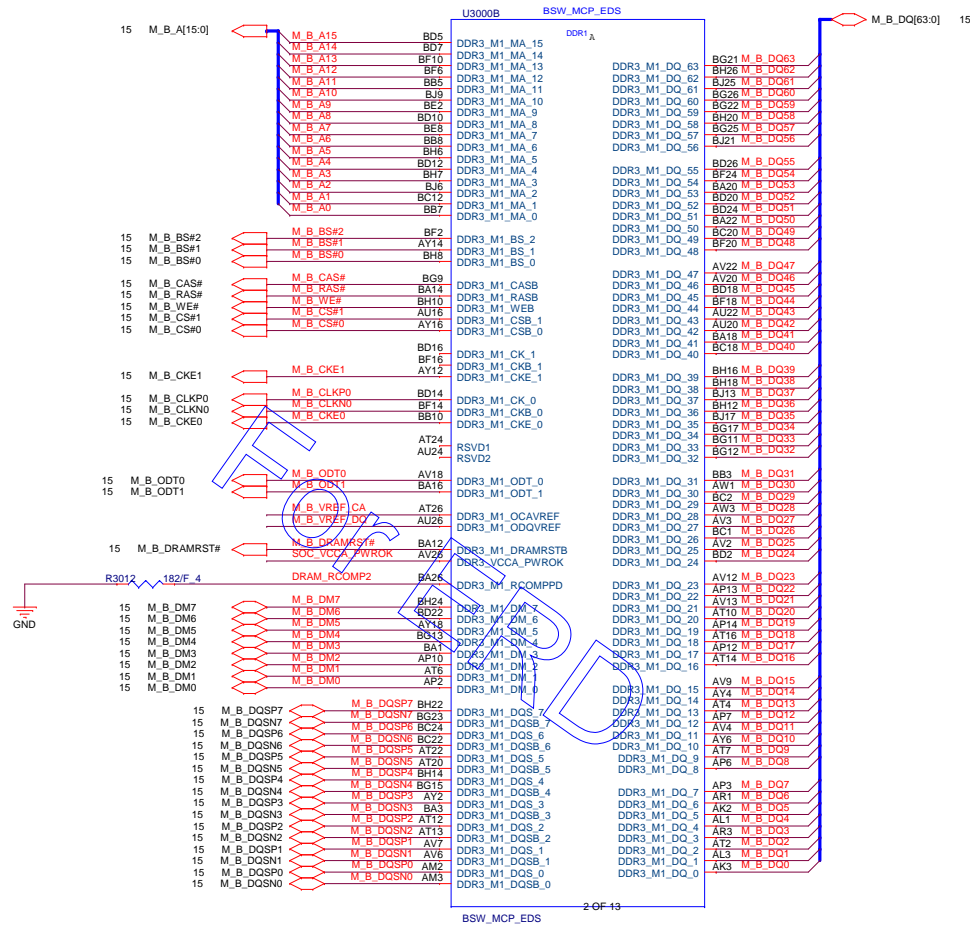
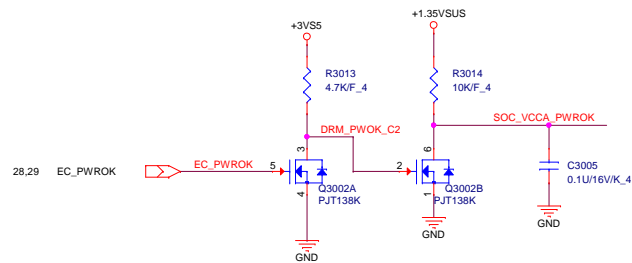
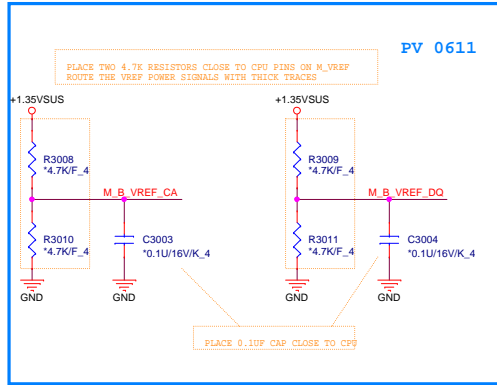
PG.24

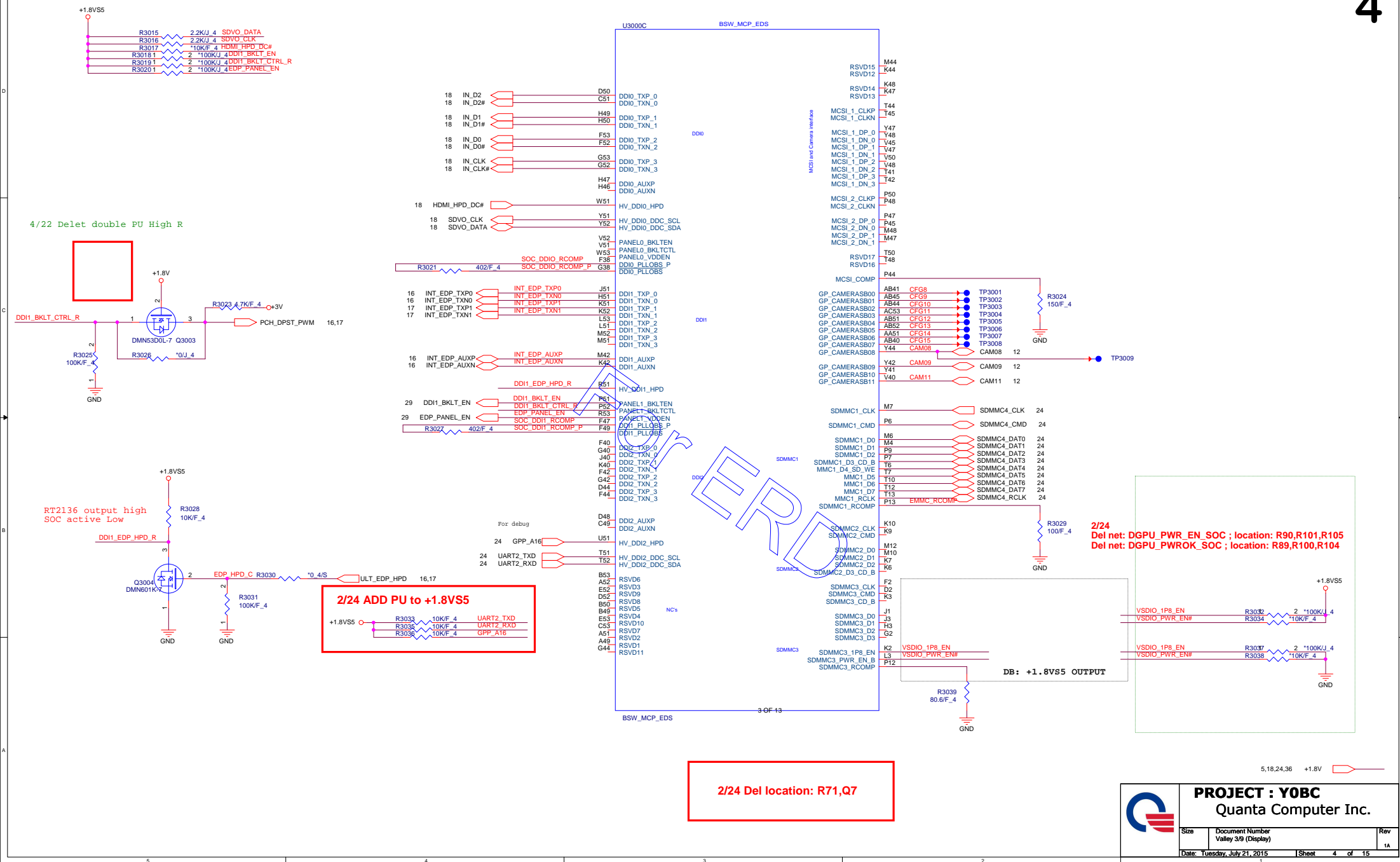


**PROJECT : YCBC**  
Quanta Computer Inc.

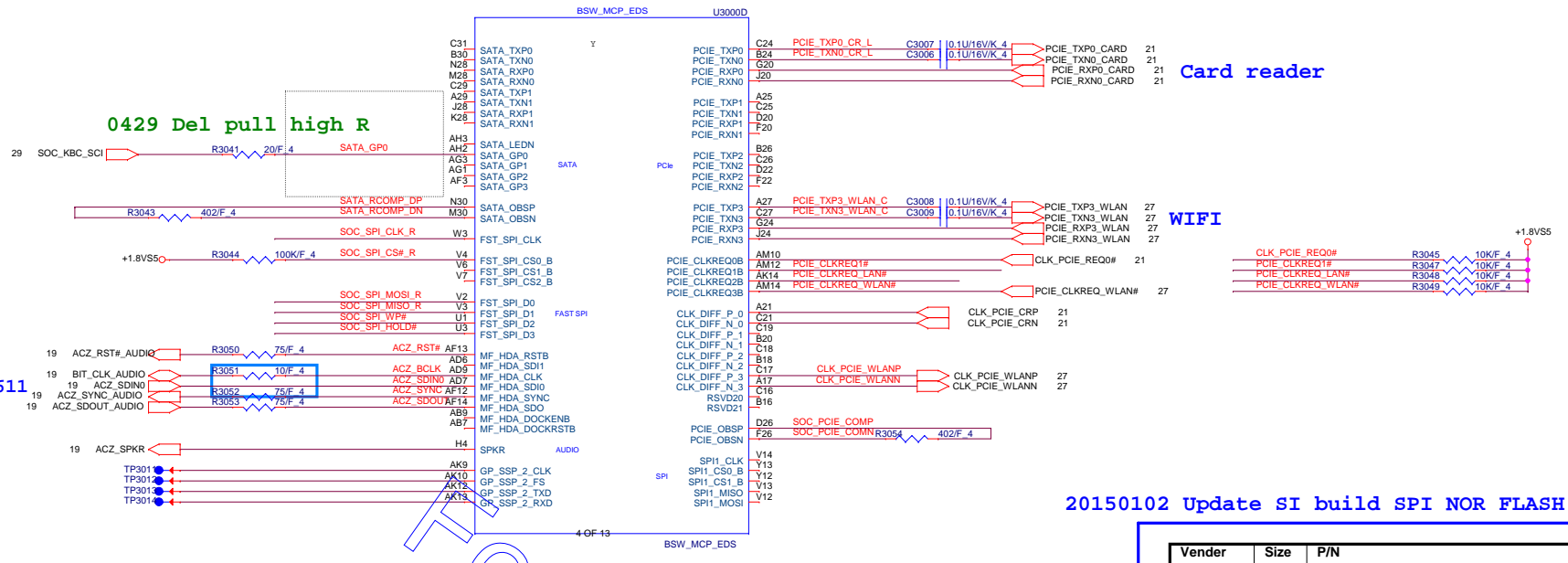
Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Tuesday, July 21, 2015	Sheet	1 of 15







HDD



Direct connect to 1.8V

To EC for share ROM

3/9 Del net: SOC\_SPL\_CLK / SOC\_SPL\_CS# / SOC\_SPL\_MISO / SOC\_SPL\_MOSI;  
location: R448,R480,R479,R462

To EC for SHPI

R3057 10/F 4 SHPI\_SPL\_CLK 28

R3058 10/F 4 SHPI\_SPL\_CS# 28

R3059 10/F 4 SHPI\_SPL\_MISO 28

R3060 10/F 4 SHPI\_SPL\_MOSI 28

SOC\_SPL\_WP# R3061 10/F 4 SHPI\_SPL\_WP# 28

SOC\_SPL\_HOLD# R3064 10/F 4 SHPI\_SPL\_HOLD# 28

From CPU

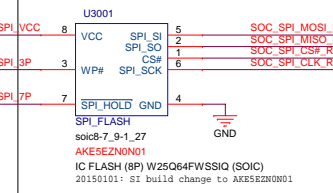
Place colay R as closed as possible  
mistach to SPI\_CLK within 250mil

0716 MV Delet socket

SPI ROM Socket

U3001 &amp; U3002 footprint 要重疊

SPI NOR FLASH



SOC\_SPL\_MOSI\_R2 TP3015

SOC\_SPL\_MISO\_R2 TP3016

SOC\_SPL\_CS#\_R2 TP3017

SOC\_SPL\_CLK\_R2 TP3018

SPI\_3P TP3019

SPI\_7P TP3020

For EMI

\*10P/50V/J C3013 SOC\_SPL\_CLK\_R2

4,18,24,36 +1.8V



**PROJECT : Y0BC**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Valley 4/9 (SD/PCIe/SATA)		1A


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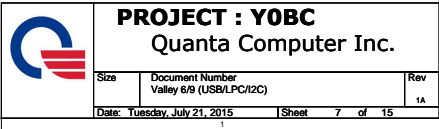


+1.8VS5

## 0605 PV change

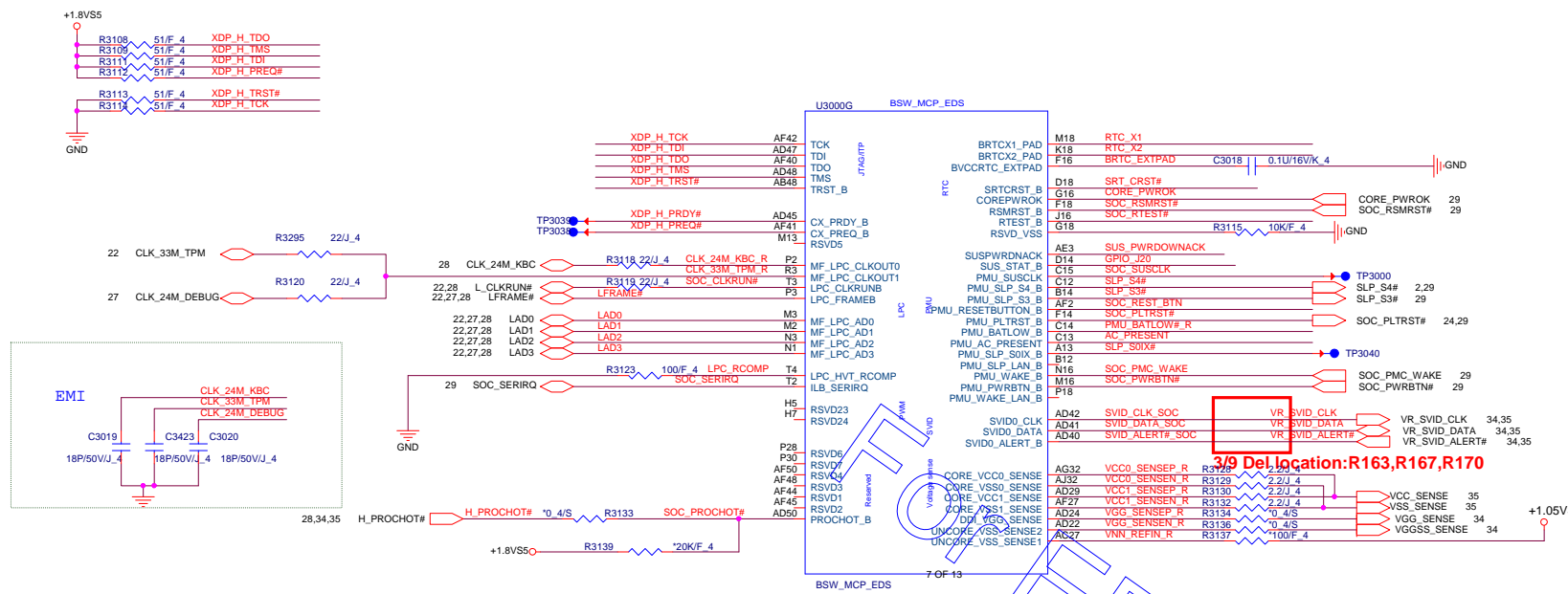
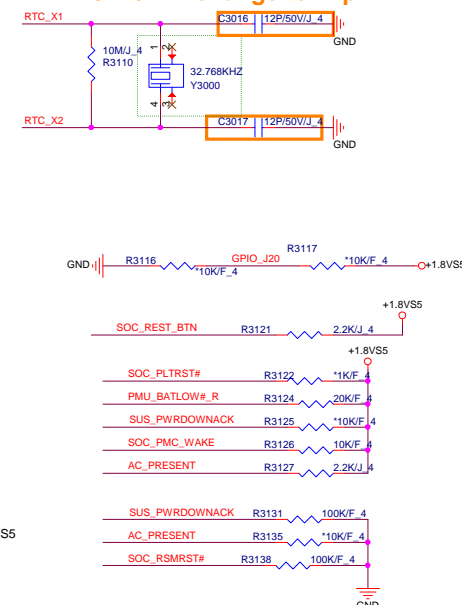
### DDR Vender Sel

	<b>PROJECT : Y0BC</b> <b>Quanta Computer Inc.</b>		
	Size	Document Number Valley 5/9 (SPUGPIO/CLK)	Rev 1A
	Date: Tuesday, July 21, 2015	Sheet	6 of 15



### RTC Clock 32.768KHz

0716 MV change to 12p



3/3 Del net: VR\_SVID\_ALERT#/VR\_SVID\_DATA/VR\_SVID\_CLK; location: R166,R42,R43,R16,R20

Close to CPU R111

Close to VCC power control PU11

Close to VGG power control PU10

### RTC Circuitry(RTC)

DTG Power trace width: 20mils

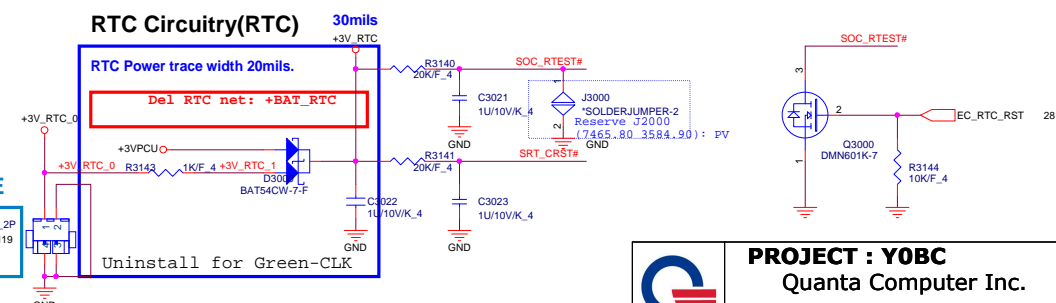
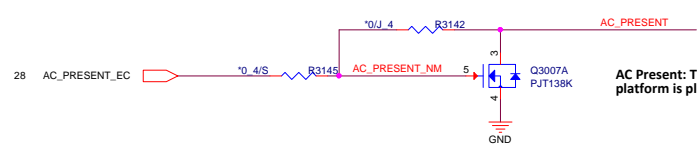
Del RTC net: +BAT\_RTC

## Uninstall for Green-CLK<sup>GN</sup>

## PV 0601 CHANGE

CN3000  
RTC\_CONN\_2P  
DFHD02MS119

**AC Present:** This input pin indicates when the platform is plugged into AC power.



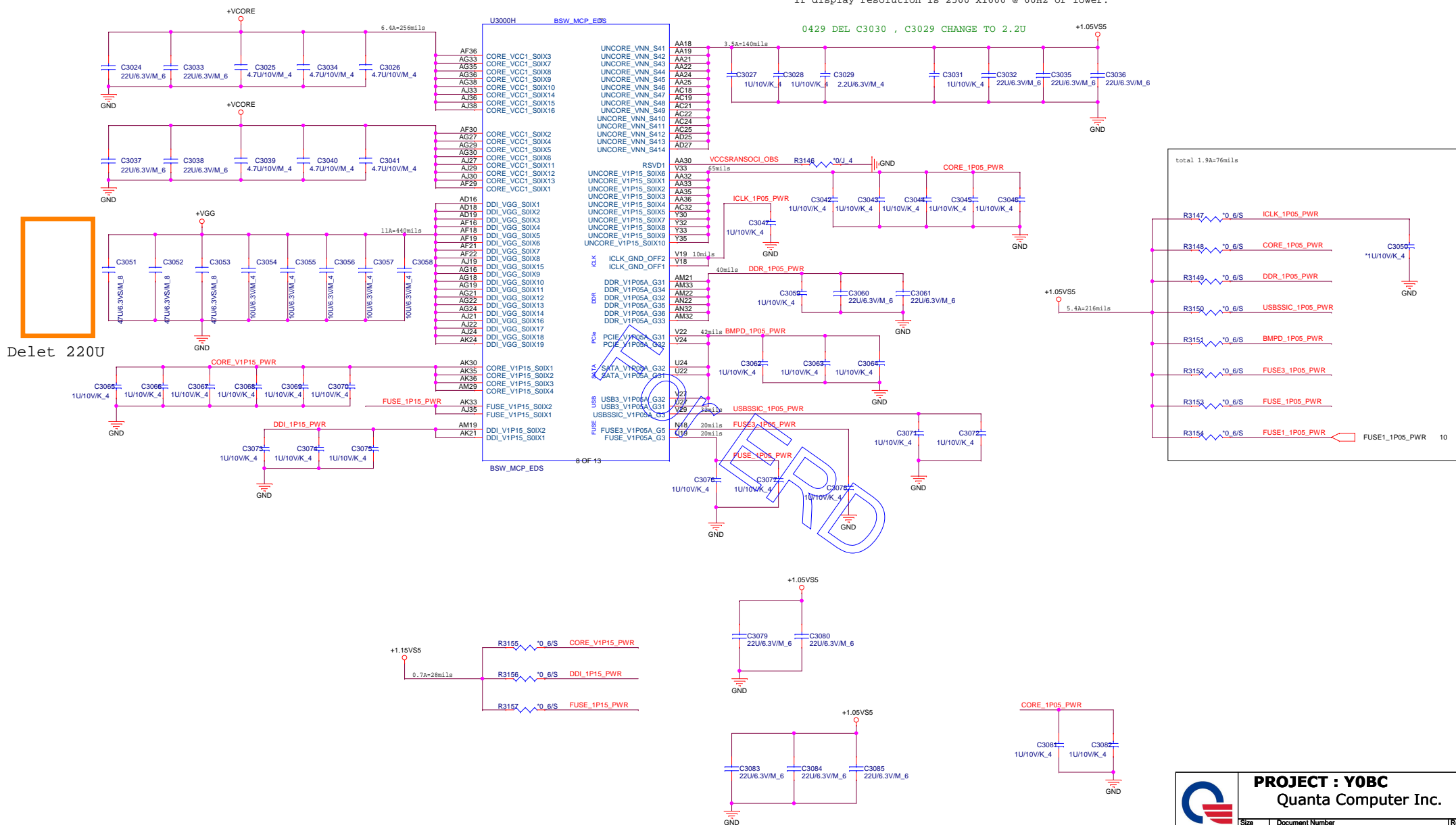
**PROJECT : Y0BC**  
Quanta Computer Inc.

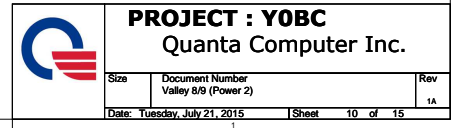
Size	Document Number Valley 6/9 (USB/LPC/I2C)	Rev 1A
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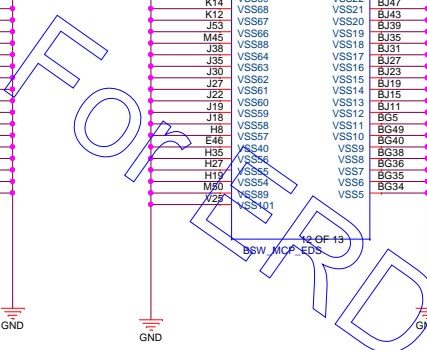


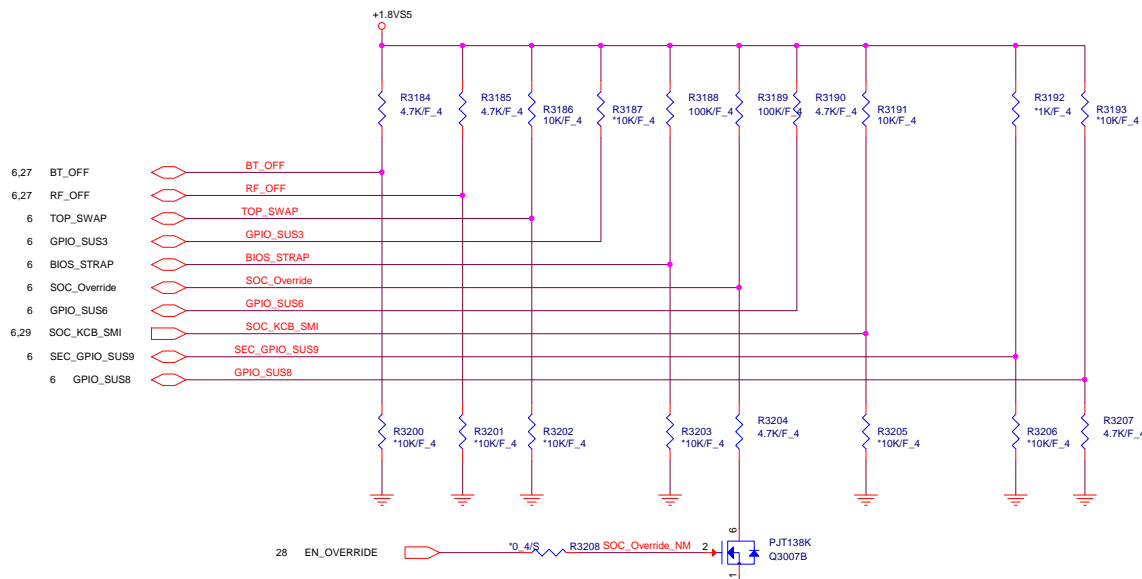
VNN can optionally be merged with V1P05A  
if display resolution is 2560 x1600 @ 60Hz or lower.

0429 DEL C3030 , C3029 CHANGE TO 2.2U

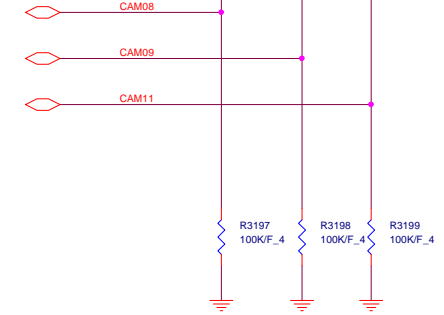









4 CAM08  
4 CAM09  
4 CAM11



	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

#### REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

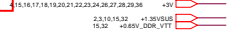
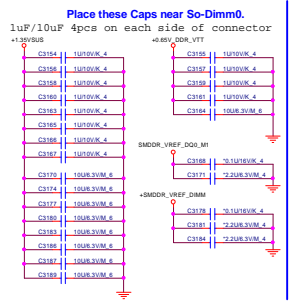
		<b>PROJECT : Y0BC</b> Quanta Computer Inc.	
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XDP <Location : CN200>

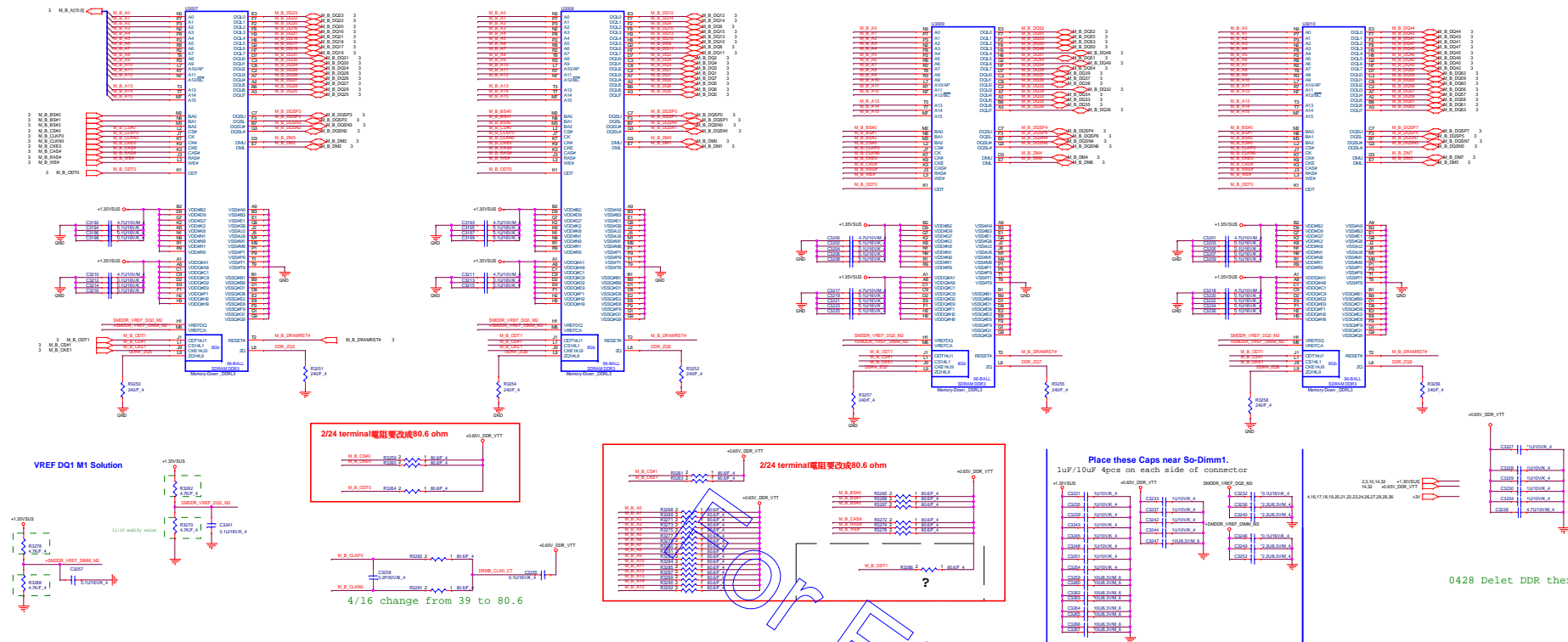
APS <Location : CN5>

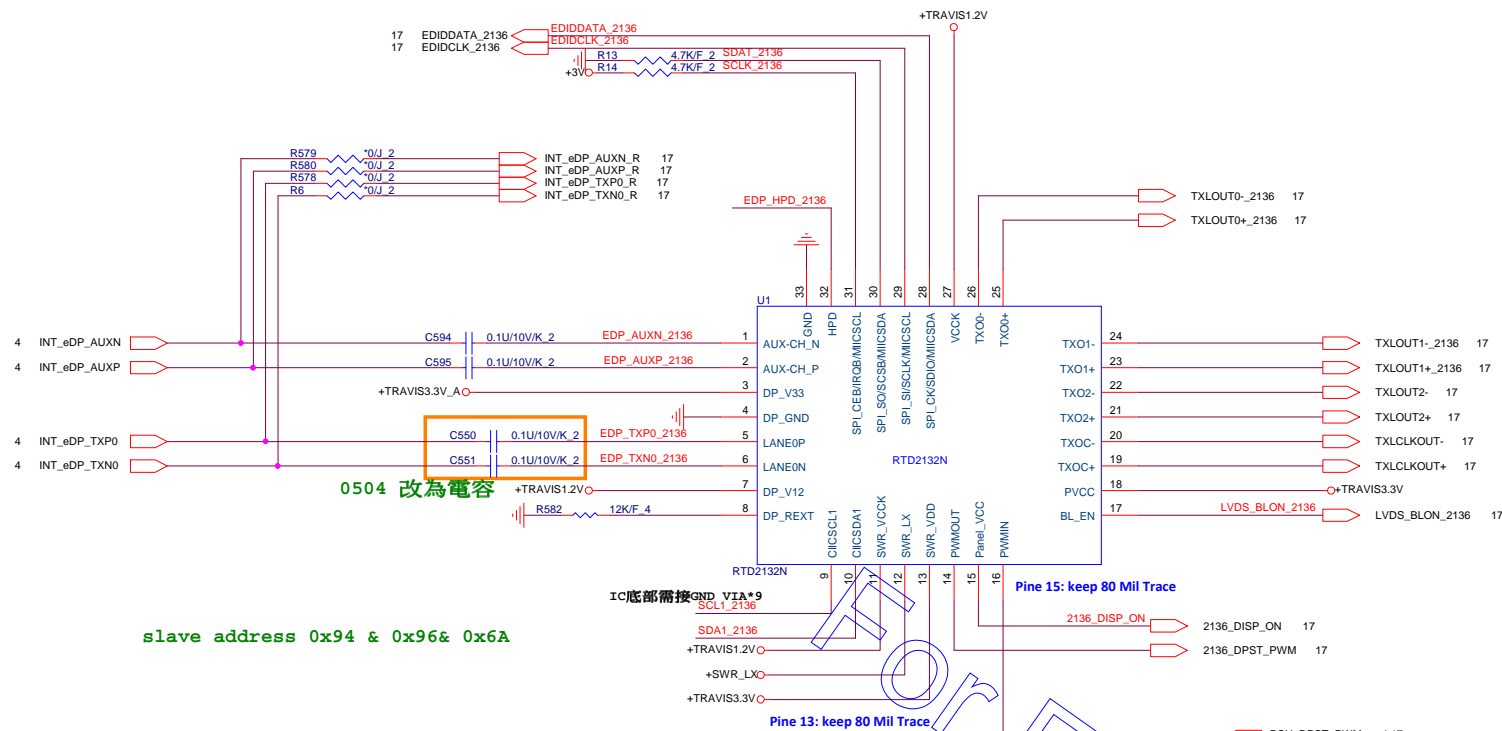
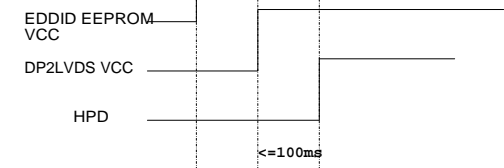
API <Location : D1,D2,Q10,U5,R119,R122,R124,R127,R179,U7>

For ERD

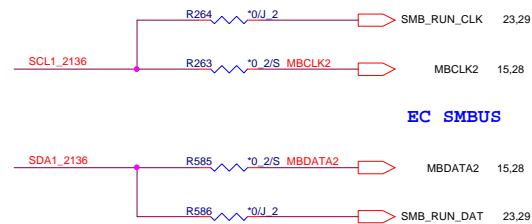
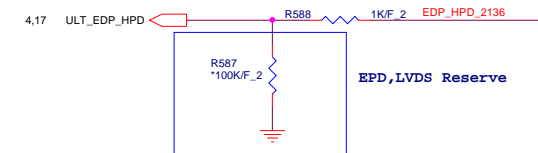


DDR3L				
TOPBS PN	QBCON	Vender PN	Description	
AKD5JGETW07	AKD5JGETW08	HSTC4G63AFR-PBA	IC SDRAM (96P) HSTC4G63AFR-PBA	Hyxos (default)
AKD5PGST568	AKD5PGST569	K4B4G1446Q-HYKO	IC SDRAM (96P) K4B4G1446Q-HYKO	Samsung
AKD5PGSTL19	K4B4G1256M16L1-Y07-N	IC SDRAM(96P)MT141256M16L1-Y07-N		micron
AKD5PGSTW14	AKD5PGSTW15	HSTC4G63CPR-PBA	IC SDRAM (96P) HSTC4G63CPR-PBA	Hyxos (NVLW Data)





```
slave address 0x94 & 0x96& 0x6A
```

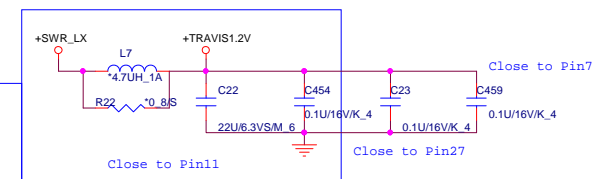
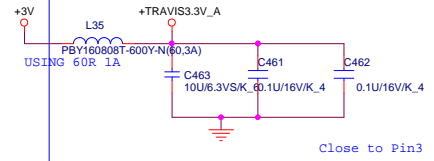
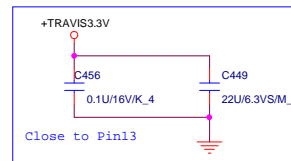
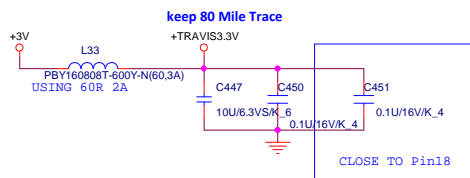


Default: ROM ONLY MODE

		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MO



L8: need use CV-4709MN00 for Vendor suggestion



SWR MODE	LDO MODE
Stuff L8	Stuff R86

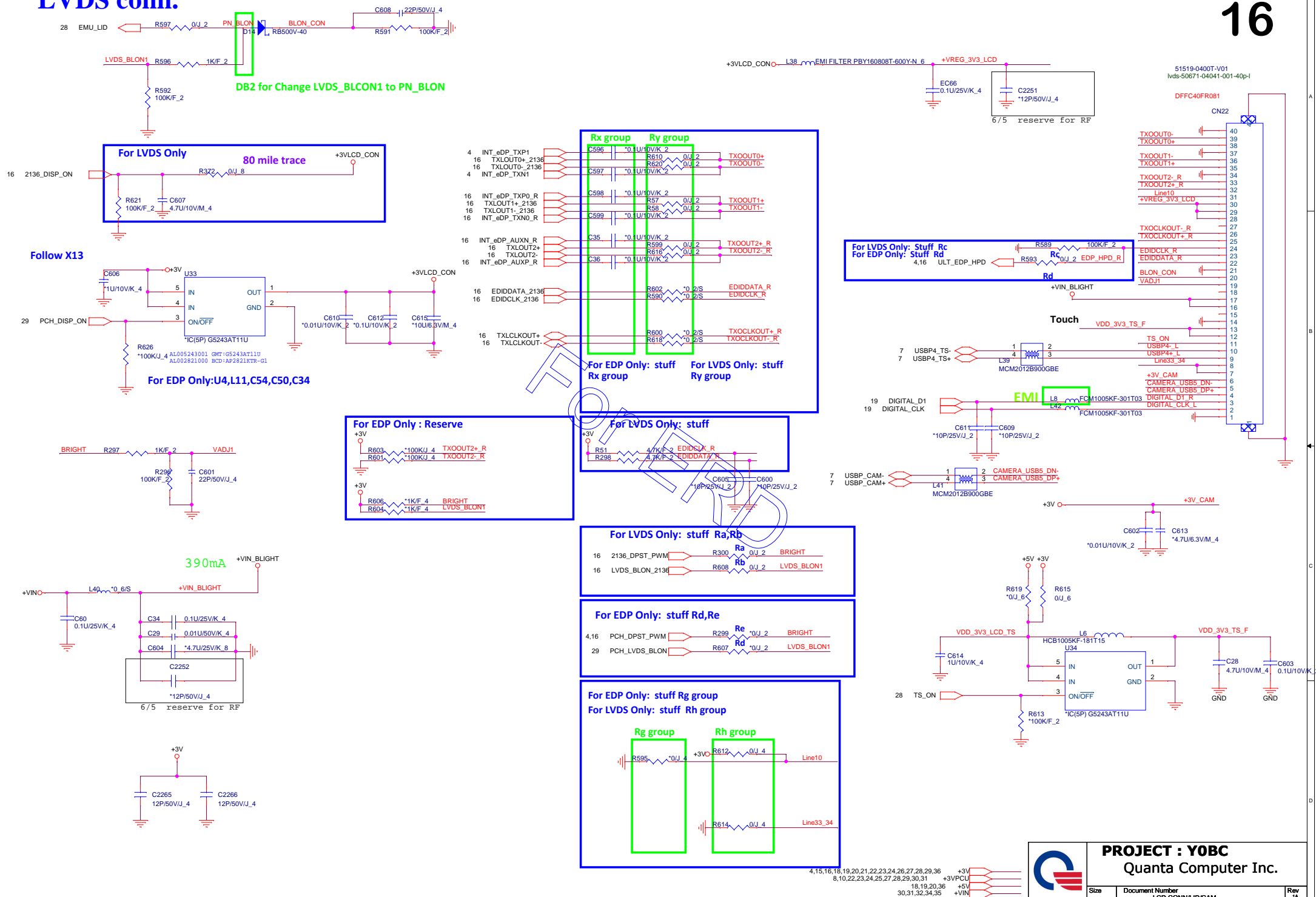


**PROJECT : Y0BC**  
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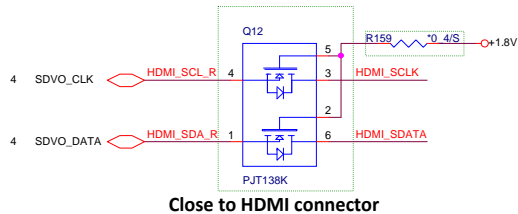


## 16



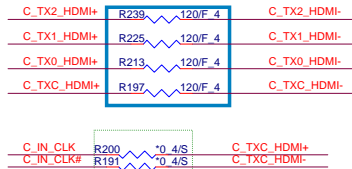
## HDMI Conn.

## HDMI SMBus Isolation

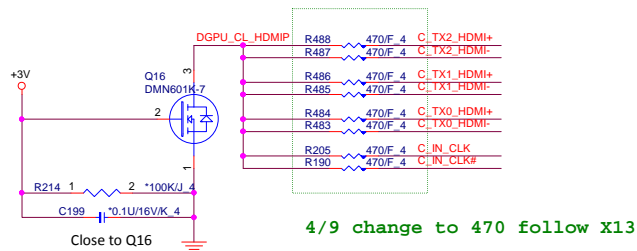
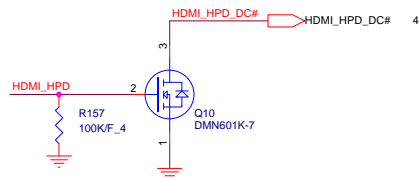


## PV 0601 Change to 120 ohm

### EMI Solution



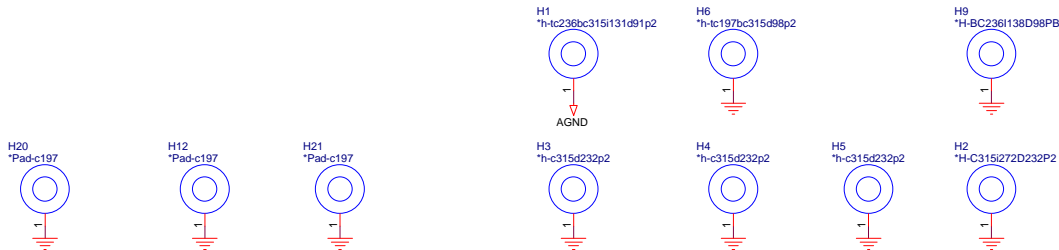
### FOLLOW W03



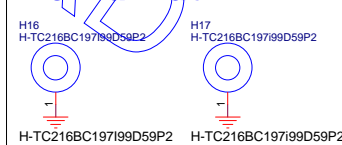
0601 short pad

for EMI request

## Hole

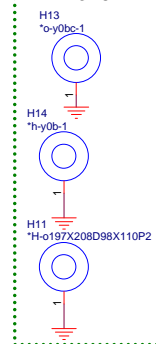


## Thermal Nut



## 11/5 Change CPU Bracket

### CPU BKT



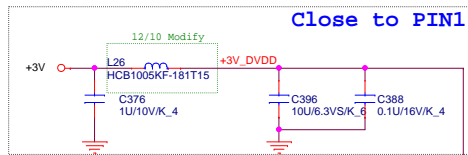
## EMI

PROJECT : Y0BC			
Quanta Computer Inc.			
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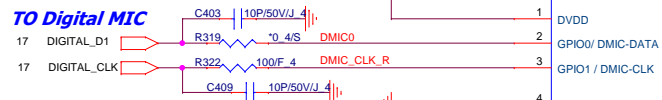
17

10/31  
modify footprint

## Close to PIN1

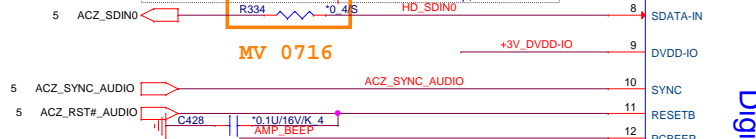


## TO Digital MIC

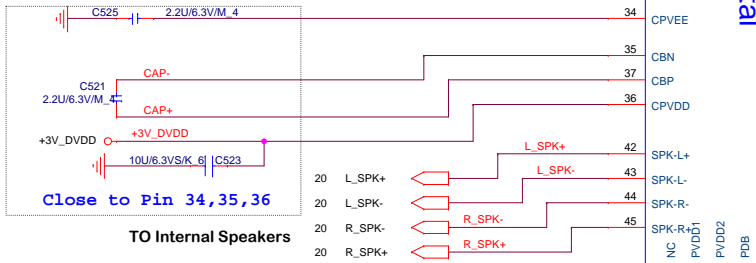


## Close to PIN7

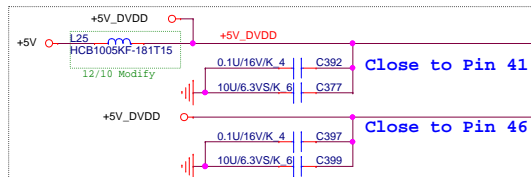
MV 0716



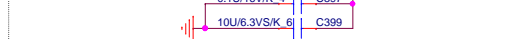
## TO Internal Speakers



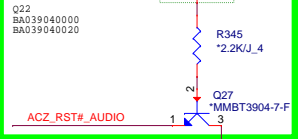
## Close to Pin 41



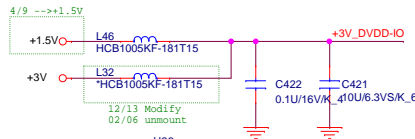
## Close to Pin 46



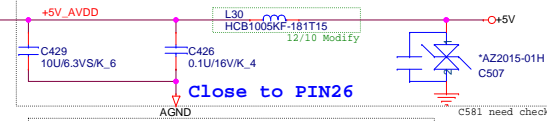
## for intel HSW ULT



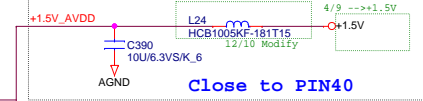
&gt;40mils trace



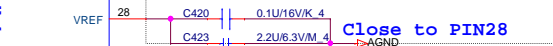
## Close to PIN26



## Close to PIN40



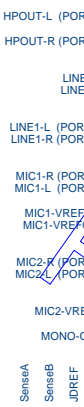
## Close to PIN28



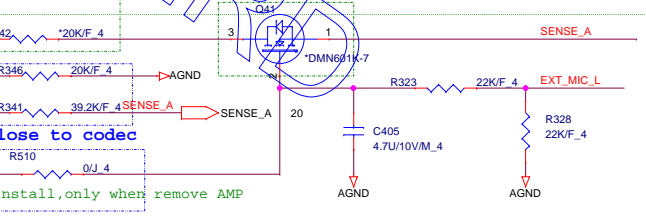
Analog

Digital

SPDIF-OUT/GPIO2

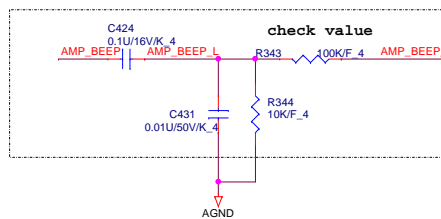


R342, Q41, R504 install, only when use AMP

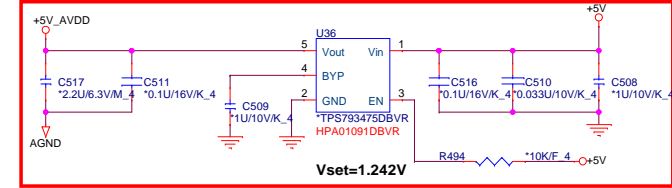


CHECK

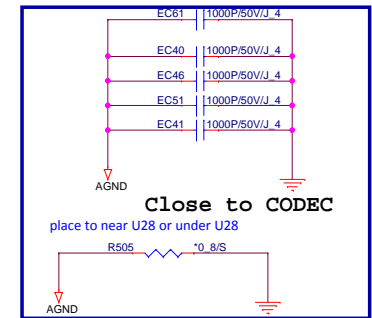
## Check layout mount location



12/24 Delete U31 and related component

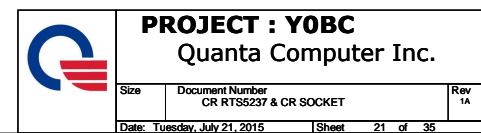


TO Combo Audio Jack MIC

12/24 change 2N7002K  
2/10 change P/N from BAN70020002 to BAN01380016Close to CODEC  
place to near U28 or under U28PROJECT : Y0BC  
Quanta Computer Inc.

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	Azalla ALC 3227	1A
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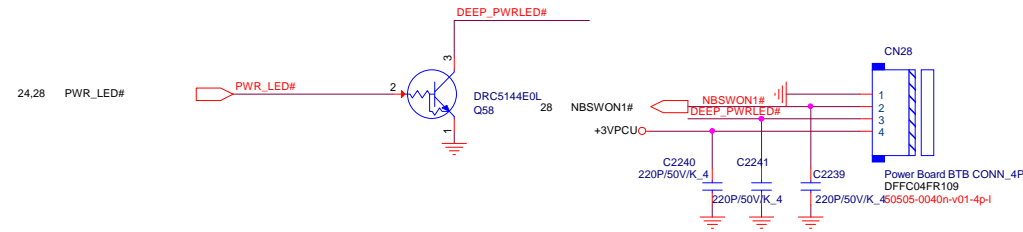




## 14" Menth Power Botton Connector

11/14 Only for debug  
12/24 Delete debug power switch

Pin1 : +3VPCU(LIDSWITCH PWR)  
Pin2 : POWER LED  
Pin3 : LIDSWITCH  
Pin4 : GND  
Pin5 : GND  
Pin6 : POWERON#

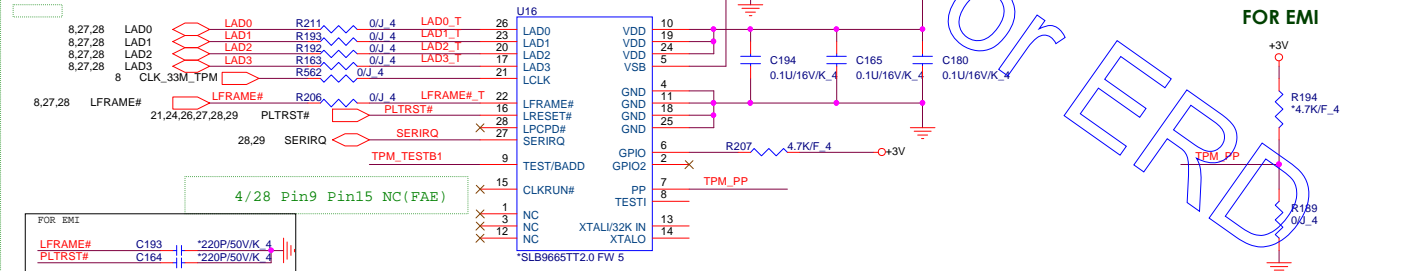


## TPM (2.0)

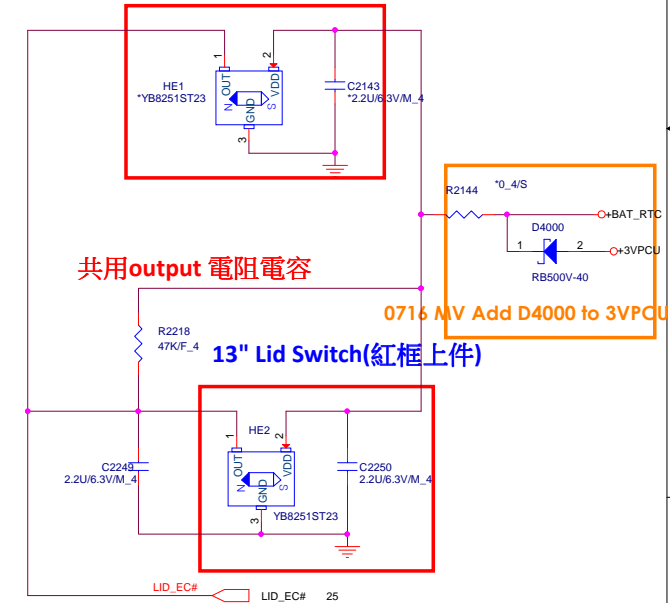
Address

	BADD
HIGH	4EH/4F (default)

5/6 R562 for LPC\_CLK 3 branches, should be 12.5ohm

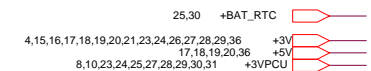


## 14" Lid Switch(紅框上件)



共用output 電阻電容

## 13" Lid Switch(紅框上件)



25,30 +BAT\_RTC

4,15,16,17,18,19,20,21,23,24,26,27,28,29,36 +3V

17,18,19,20,36 +5V

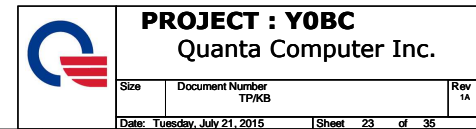
8,10,23,24,25,27,28,29,30,31 +3VPCU

**PROJECT : Y0BC**  
Quanta Computer Inc.

Size Document Number TPM/TP/FAN/LED Rev 1A

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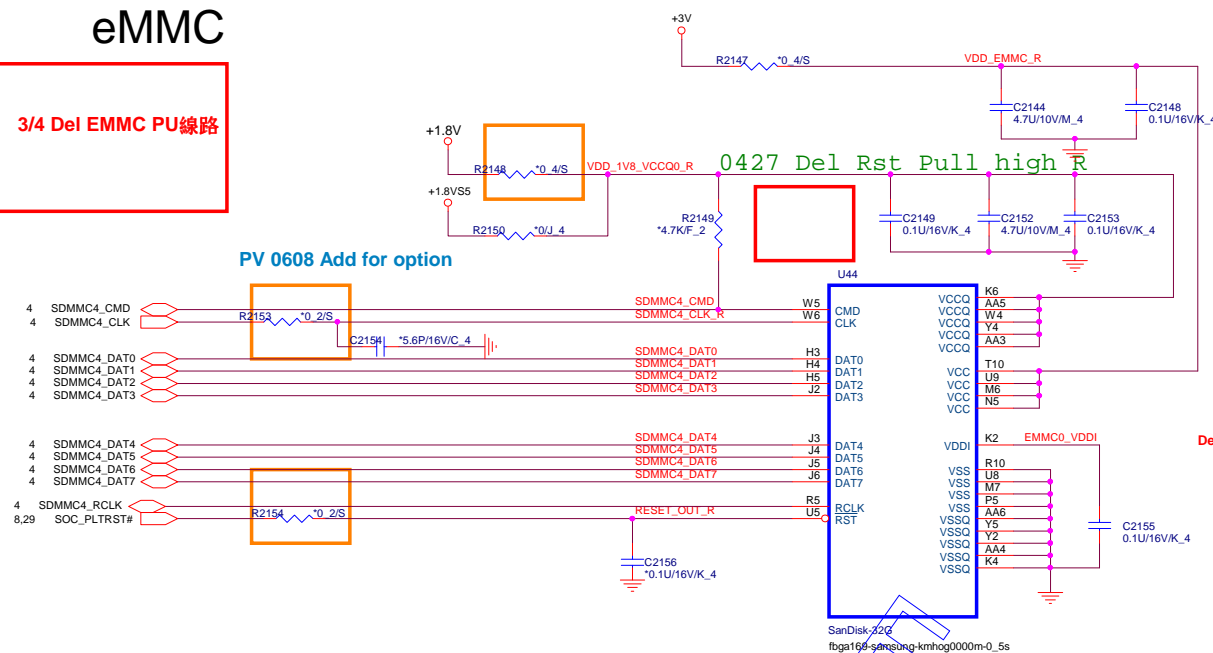


# eMMC

3/4 Del EMMC PU線路

4/27 modify cap value follow FAE

PV 0608 Add for option



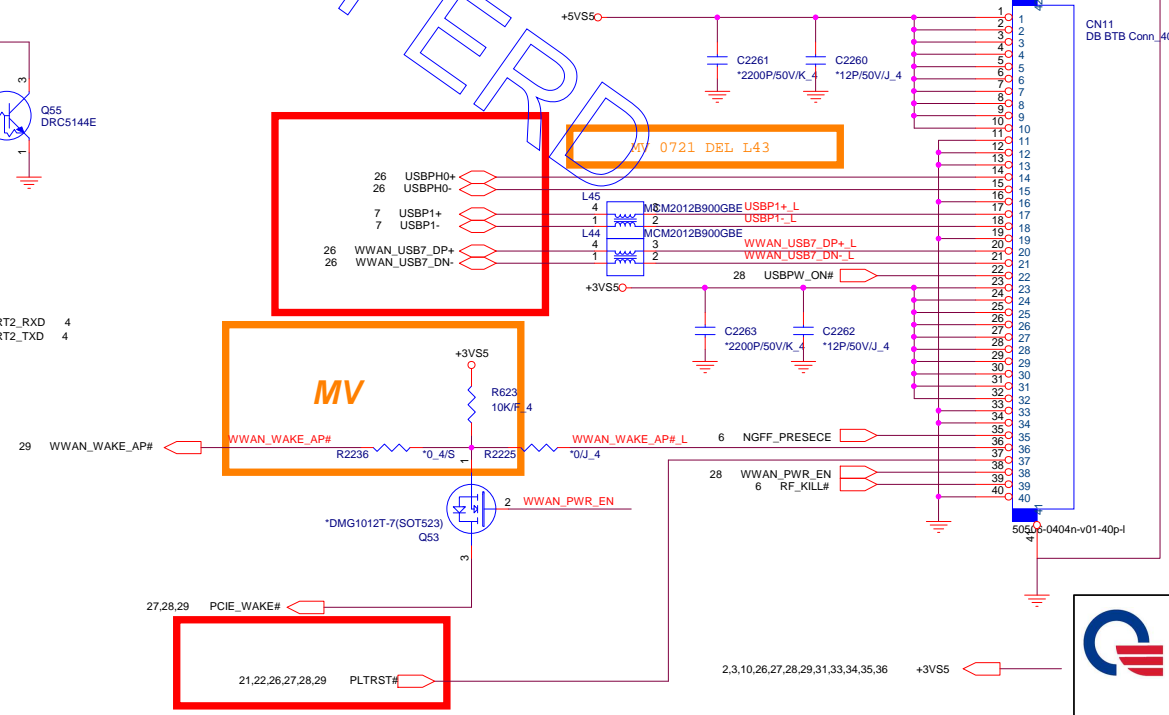
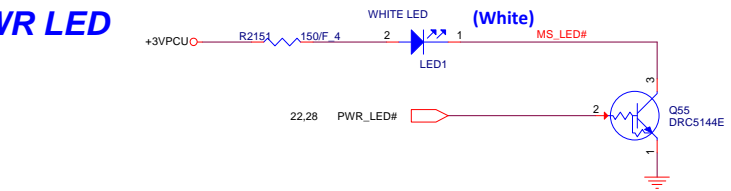
Default


iNAND (eMMC) V4.51				
TOPBSQ	QBCON	Description	SIZE	Vender
AKE3SZ-TW01	AKE3SZ-TW02	IC FLASH(153P)H26M64103EMR(FBGA)	32G	Hynix
AKE5SZ0T506	AKE5SZ0T507	IC FLASH(153P)KLMBG4GEAC-B031(BGA)	32G	samaung
AKE3SFUT000	AKE3SFUT001	IC FLASH(153P)SDIN9DW4-32G(FBGA)	32G	SanDisk
AKE3TG-TW01	AKE3TG-TW02	IC FLASH(153P)H26M78103CCR(FBGA)	64G	Hynix
AKE3TZPT515	AKE3TZPT516	IC FLASH(153P)KLMCG8GEAC-B031(BGA)	64G	samaung
AKE3TFUT101	AKE3TFUT102	IC FLASH(153P)SDIN9DW4-64G(FBGA)	64G	SanDisk

SanDisk 22G  
ftga169-samsung-kmhog0000m-0\_5s  
footprint : BGA 169 - BGA 153 co-lay  
BGA 169 PIN : 14mmX13mm  
BGA 169 PIN : 12mmX16mm  
BGA 153 PIN : 11.5mmX13mm

## PWR LED

## UART for DEBUG



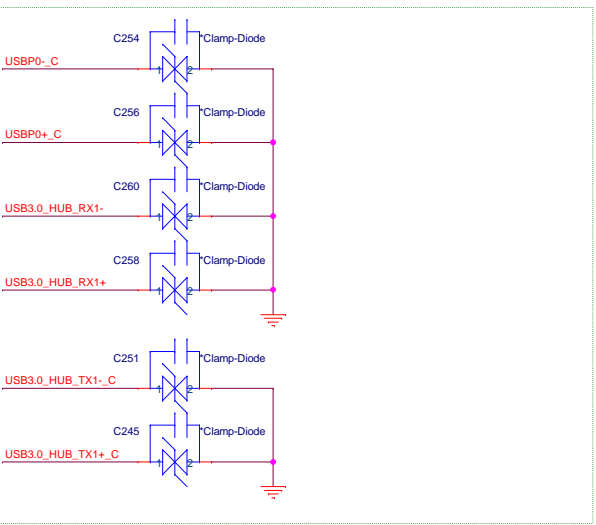


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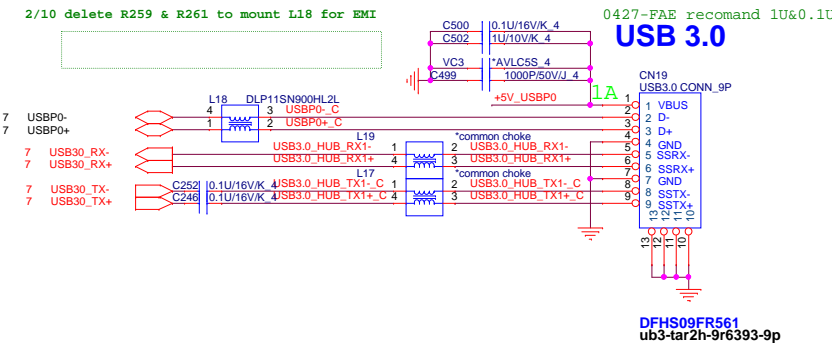
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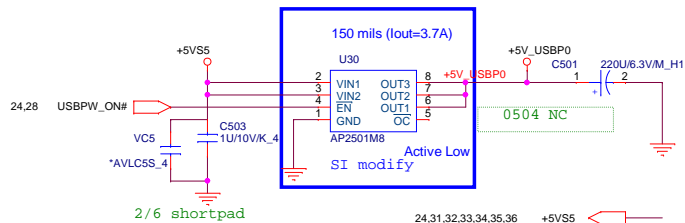
# USB 2.0/3.0 Combo



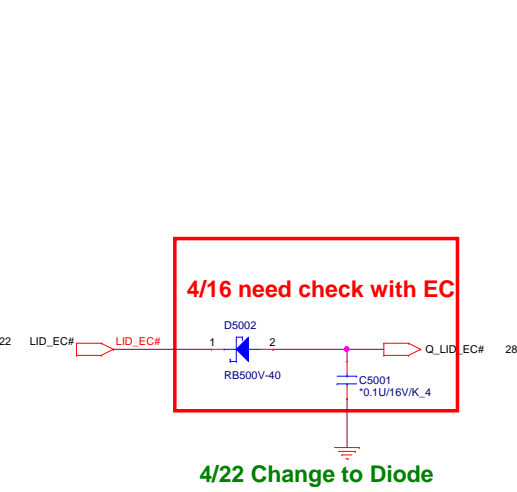
11/1 modify



## USB 3.0

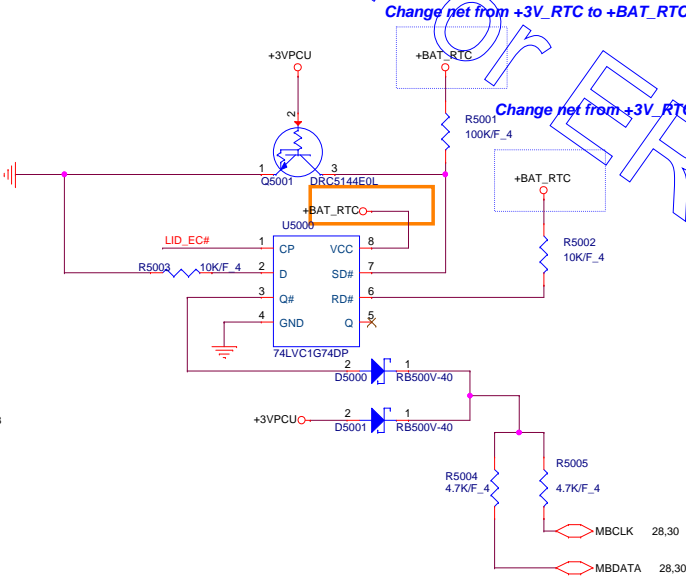


## Storage mode



4/16 need check with EC

4/22 Change to Diode



Change net from +3V\_RTC to +BAT\_RTC

Change net from +3V\_RTC to +BAT\_RTC

Input				Output	
SD	RD	CP	D	Q	Q̄
H	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

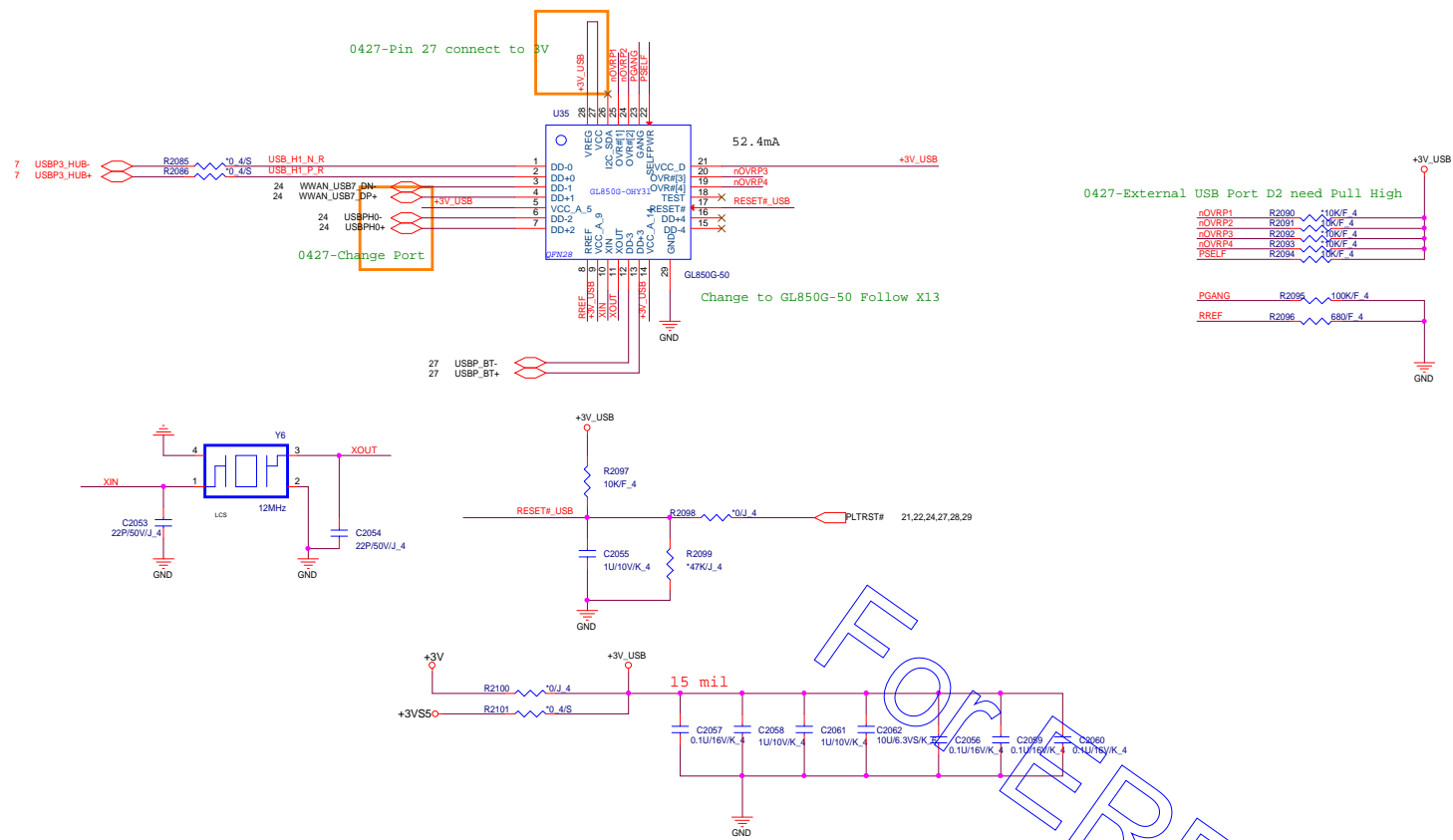
Input				Output	
SD	RD	CP	D	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
Q<sub>n+1</sub> = state after the next LOW-to-HIGH CP transition.

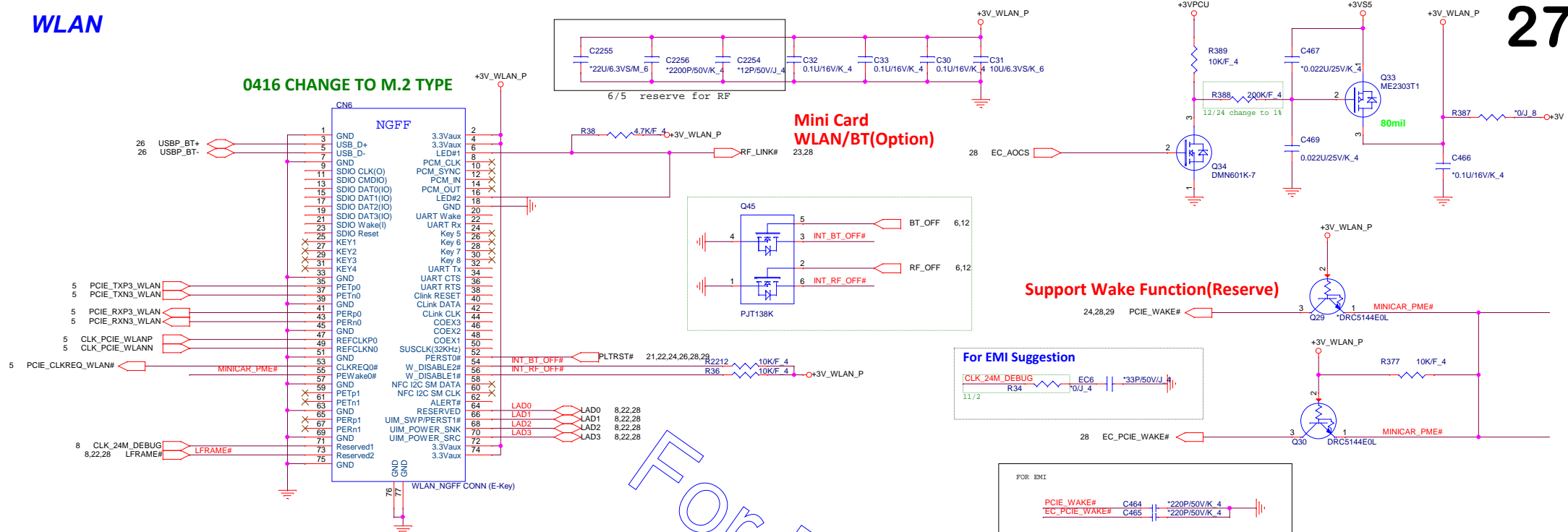


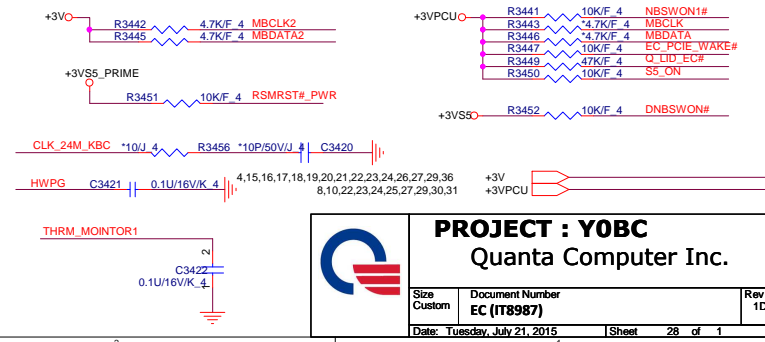
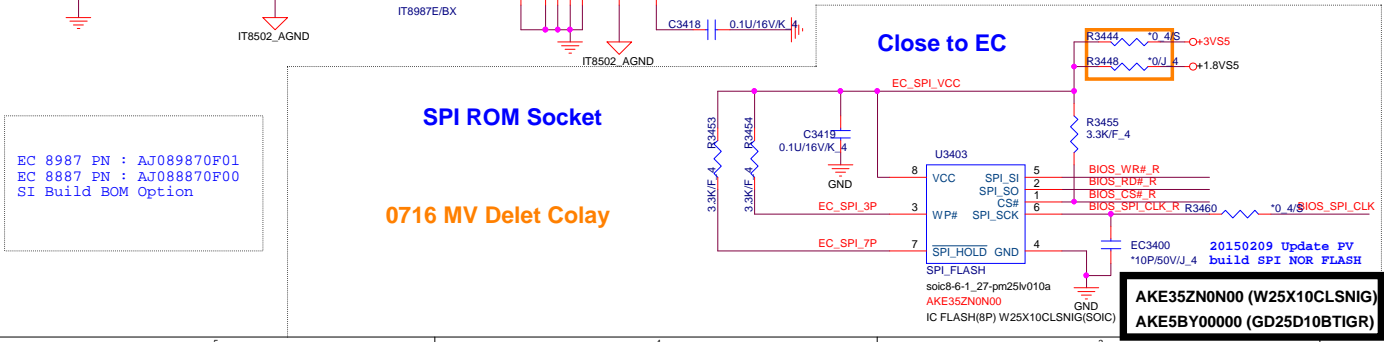
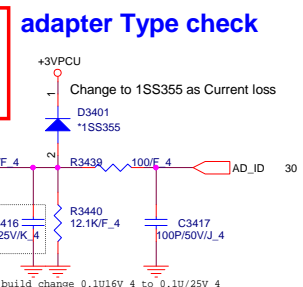
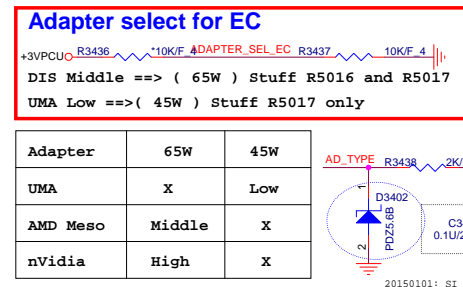
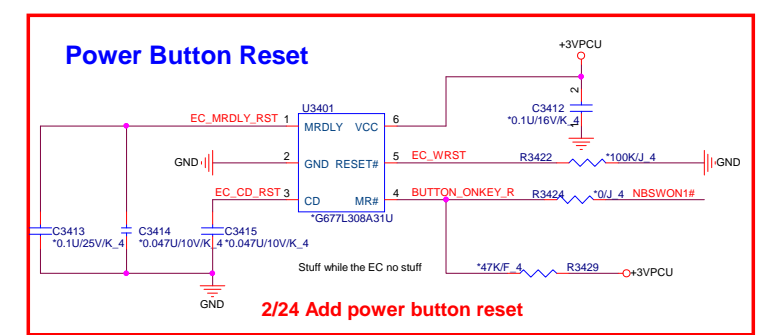
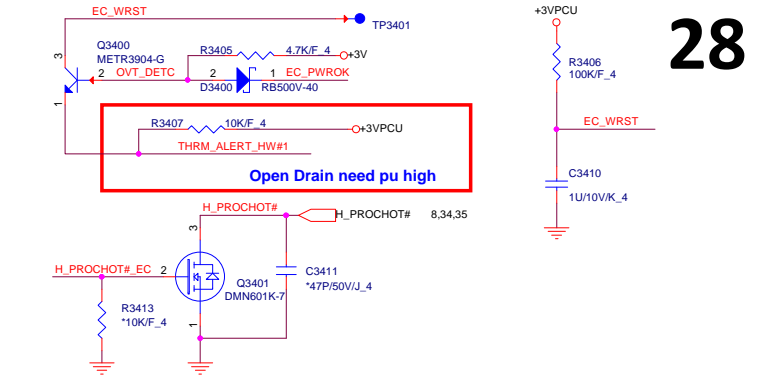
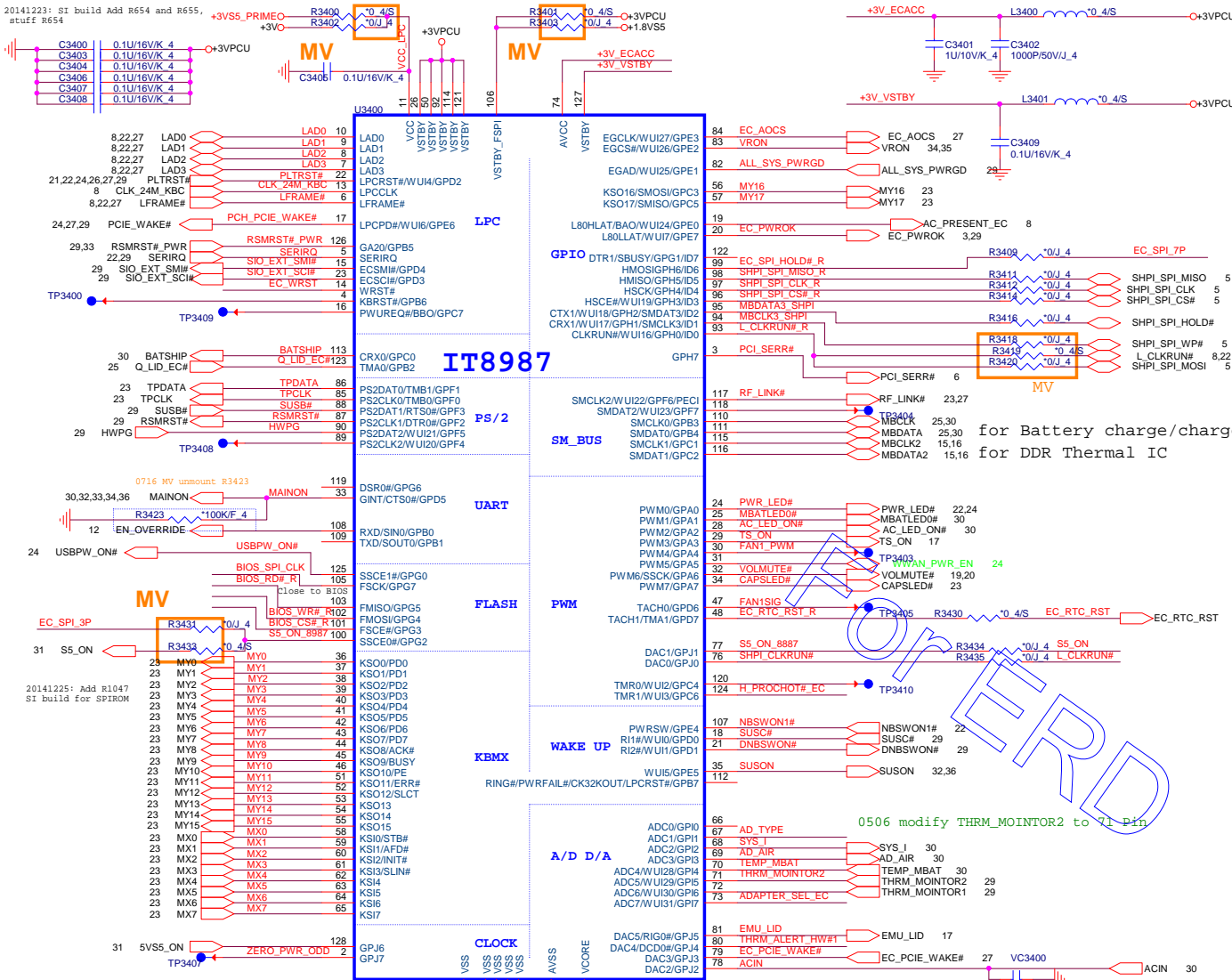
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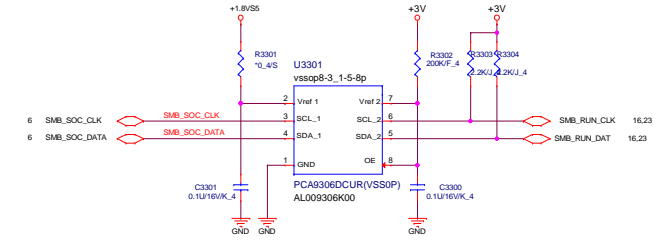
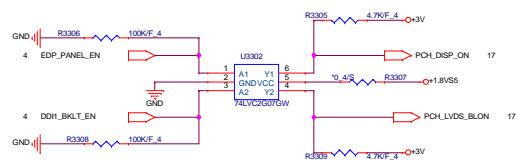
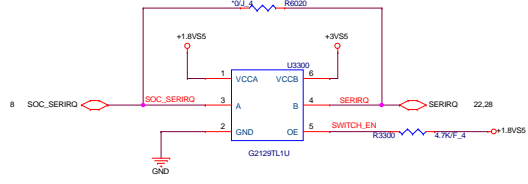


0416 CHANGE TO M.2 TYPE

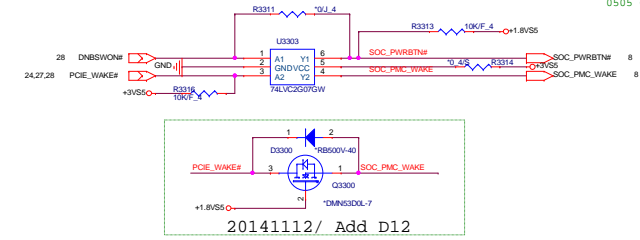




0506 Reserve for EC



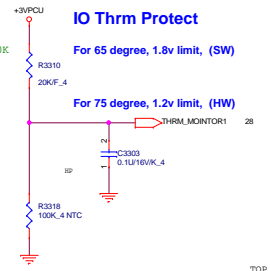
0506 NEED CHECK WITH EC AGAIN



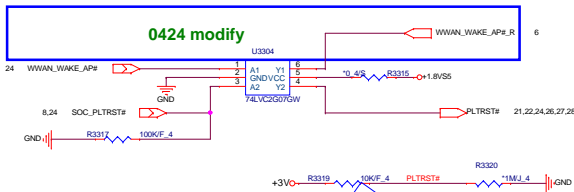
IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

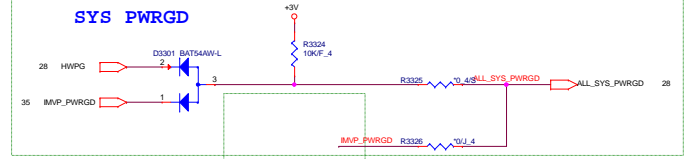
For 75 degree, 1.2v limit, (HW)



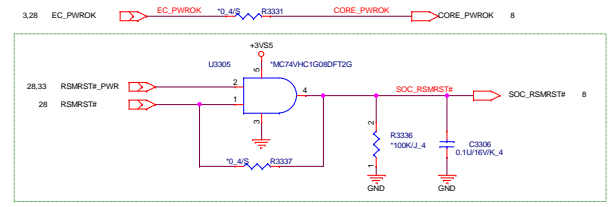
0424 modify



SYS PWRGD



Delet C358 follow X13



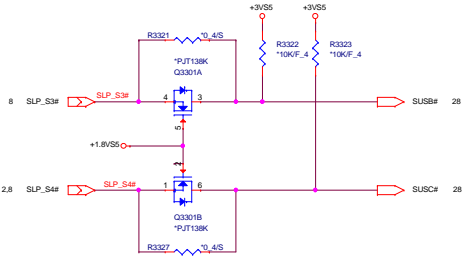
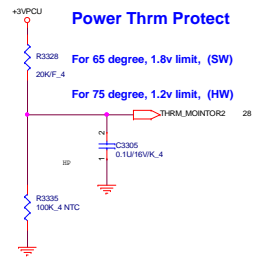
11/5 Add AND gate

Power Thrm Protect

For 65 degree, 1.8v limit, (SW)

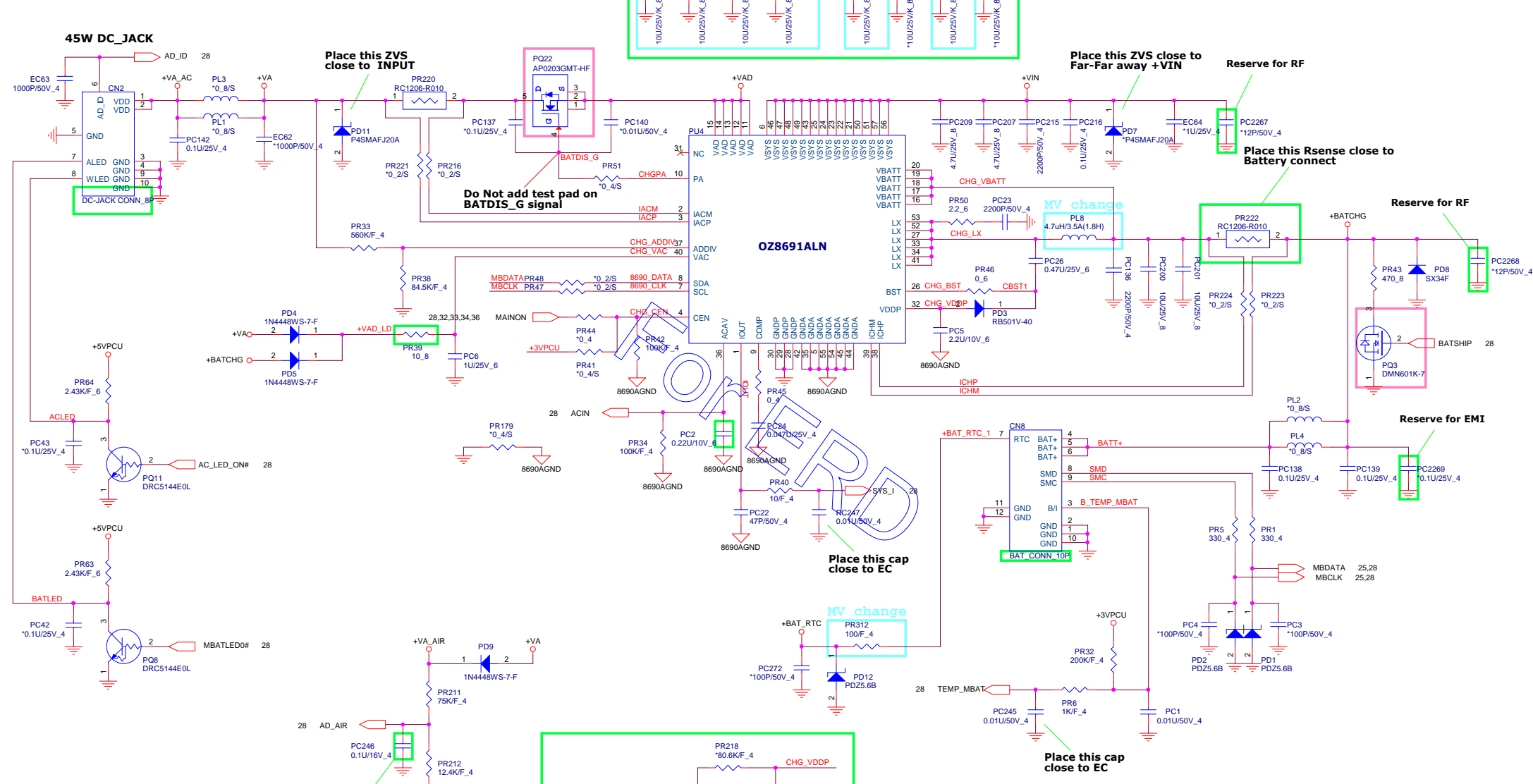
For 75 degree, 1.2v limit, (HW)

0505 CHANGE TO 20K



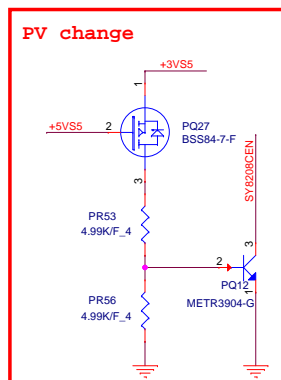
Follow X13  
No-stuff: U3306  
Stuff: R3333 R3338

Pull high in CPU side



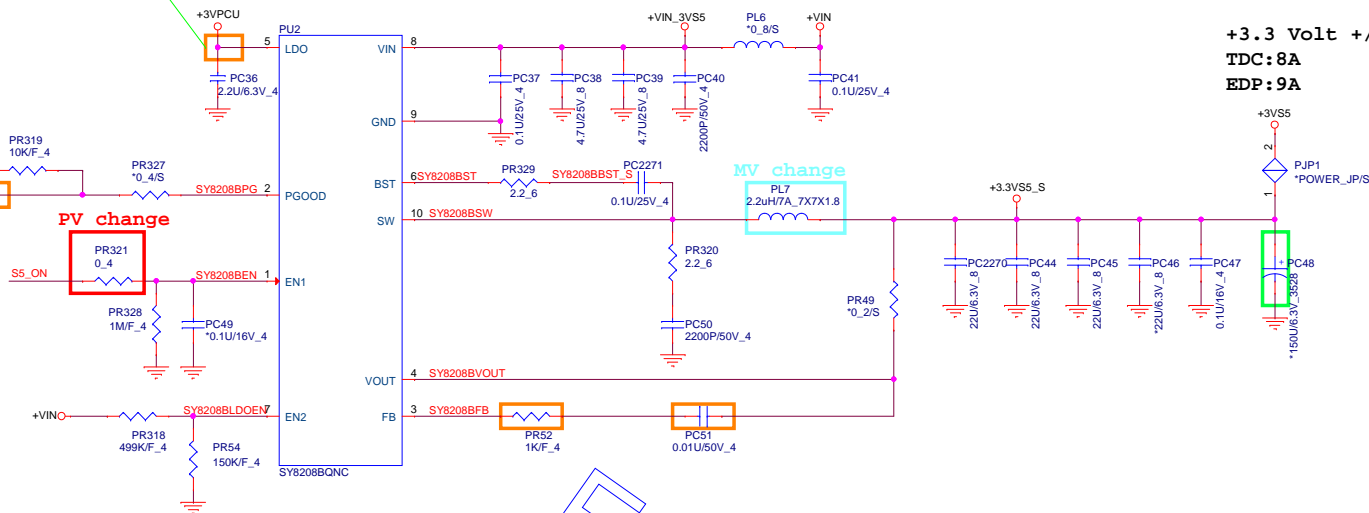
+3VS5 2,3,10,24,26,27,28,29,33,34,35,36  
+5VS5 24,25,32,33,34,35,36

Do Not add test pad on VCC & LDO pin



Auto-recover PU11 latch

**PV change**

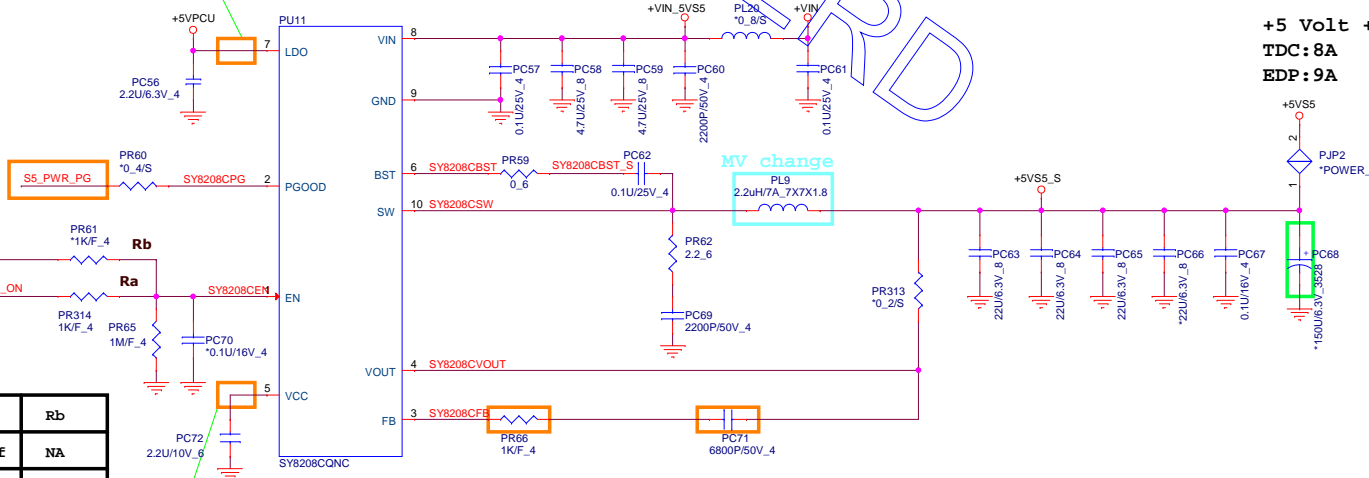


**+3.3 Volt +/- 5%**  
**TDC:8A**  
**EDP:9A**

Do Not add test pad on VCC & LDO pin

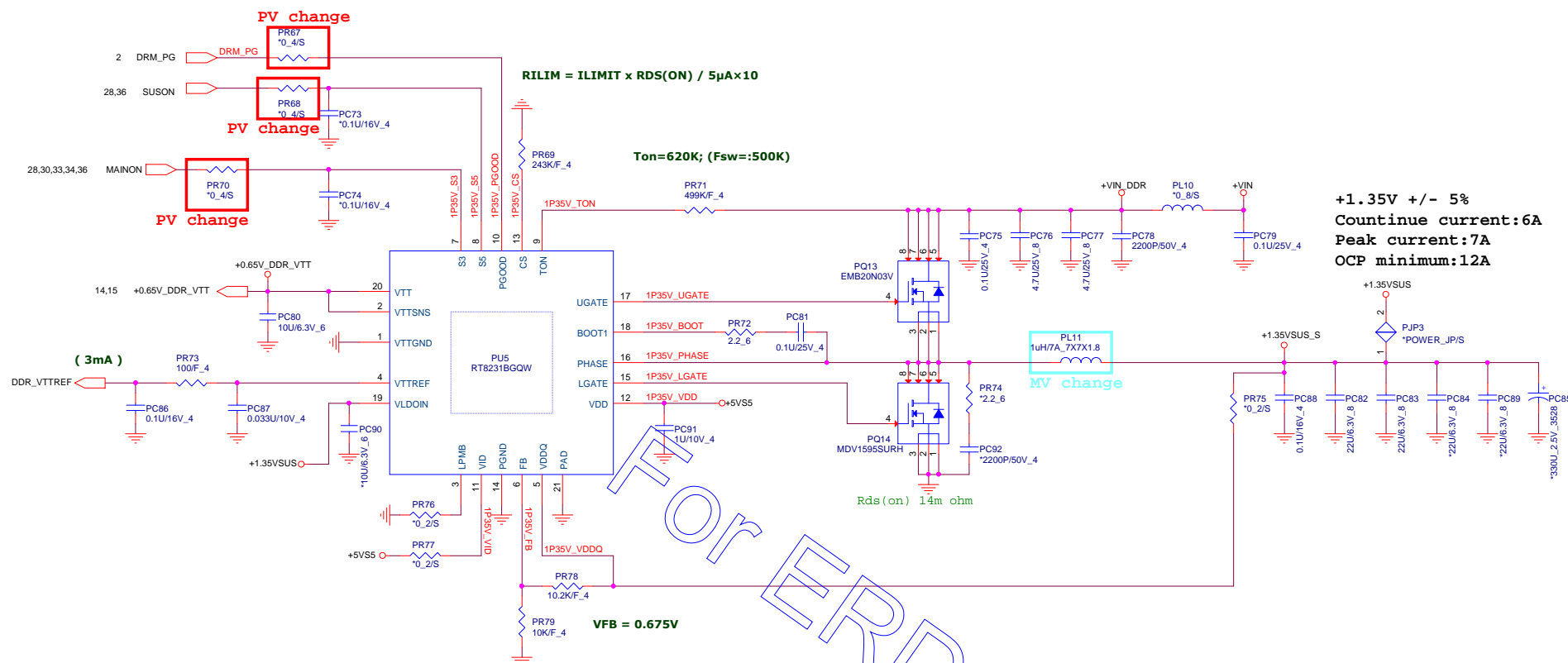
Reserve for USB Charge

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff



**+5 Volt +/- 5%**  
**TDC:8A**  
**EDP:9A**

Do Not add test pad on VCC & LDO pin



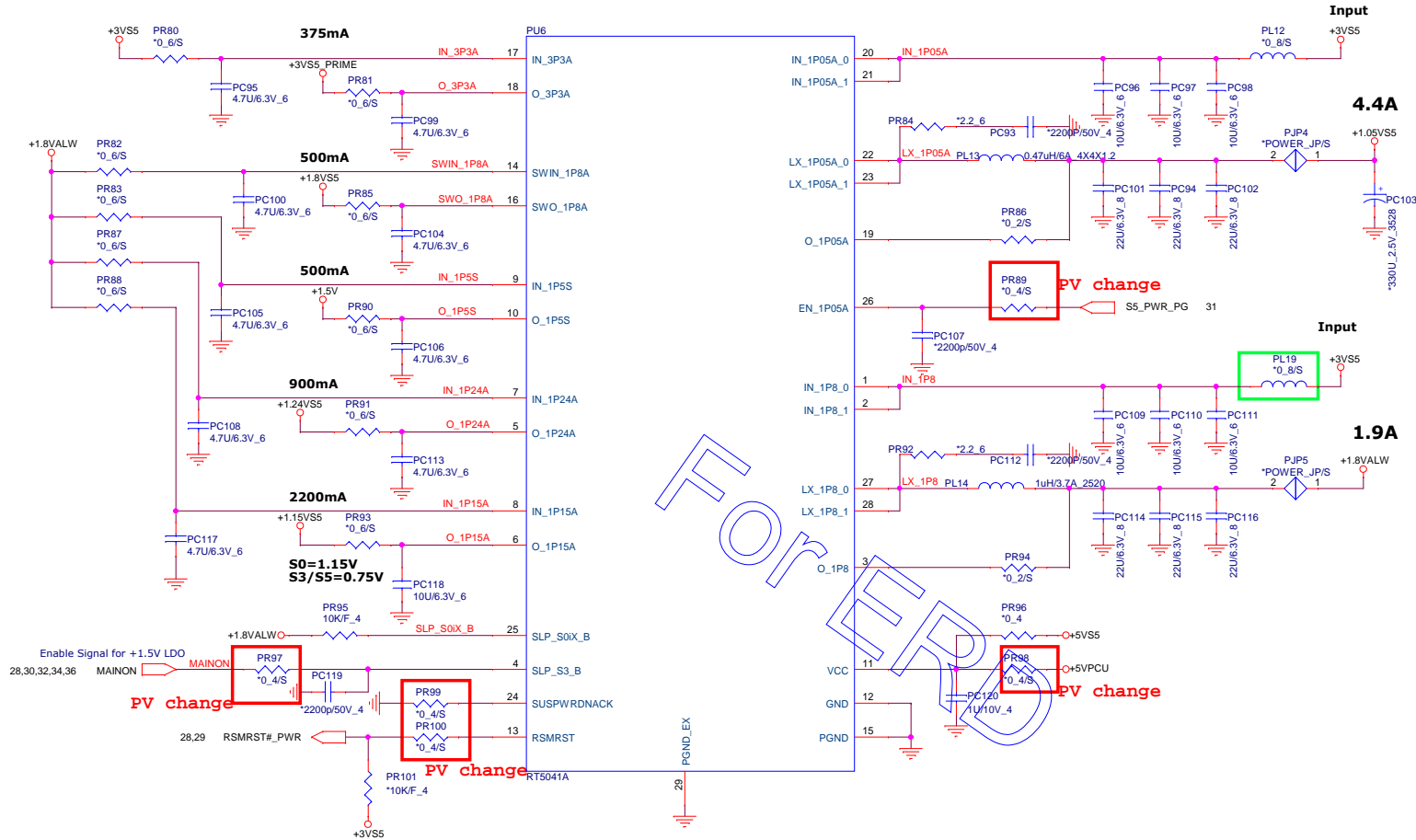
 +1.35VSUS 2,3,10,14,15



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+3VS5	2,3,10,24,26,27,28,29,31,34,35,36
+1.8VALW	36
+1.8VS5	4,5,6,7,8,10,12,28,29,34
+3VS5 PRIME	10,28
+1.5V	10,19
+1.24VS5	10
+1.15VS5	9,33
+5VPCU	30,31,33
+1.05VS5	8,9,34,35
+1.8V	4,5,18,24,36

+3VS5 2,3,10,24,26,27,28,29,31,33,35,36  
 +1.05VS5 8,9,33,35  
 +5VS5 24,25,31,32,33,35,36  
 +VGG 9  
 +1.8VS5 4,5,6,7,8,10,12,28,29,33  
 +VIN 17,30,31,32,35

